EAST - [10065187.wsp:1]

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L3: (5) test and deep adj
L3: (105) deep adj trench
L4 (3) 3 and substrate a
L5: (3) 3 and substrate a
L6: (55) 3 and substrate
L8: (3) 3 and substrate a
L9 (46) 3 and substrate
L10: (43) 3 and substrate

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DBs USPAT,EPO,JPO

Default operator: OR

Highlight all occurrences initially

deep adj trench adj capacitor and word adj line$1

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	U	1	Document ID	Issue Date	Pages	Title	Current OR	Current XRef
38	☑	☐	US 6040210 A	20000321	67	3F-square memory cell for gigabit memory applications	438/239	257/E27.084; 257/E21.654;
39	☑	☐	US 6037194 A	20000314	37	Method for making a DRAM cell with grooved transfer	438/147	438/171
40	☑	☐	US 6034389 A	20000307	69	Self-aligned diffused source vertical transistors with	257/301	257/906; 257/908;
41	☑	☐	US 6033967 A	20000307	8	Method for increasing capacitance in DRAM	438/398	438/255
42	☑	☐	US 6033957 A	20000307	70	1F square memory cell having vertical floating-gate	438/270	257/E27.103; 257/E29.129;
43	☑	☐	US 6025245 A	20000215	7	Method of forming a trench capacitor with a sacrificial	438/386	438/243
44	☑	☐	US 6016268 A	20000118	11	Three transistor multi-state dynamic memory cell for	365/149	365/174
45	☐	☐	US 6013548 A	20000111	70	Self-aligned diffused source vertical transistors with	438/242	257/E27.091; 438/243;
46	☐	☐	US 5998821 A	19991207	19	Dynamic ram structure having a trench capacitor	257/301	257/296; 257/302;
47	☑	☐	US 5998820 A	19991207	16	Fabrication method and structure for a DRAM cell	257/296	257/296; 257/302;
48	☑	☐	US 5998410 A	19991130	7	Multiplication of storage capacitance in memory cells	365/149	365/210;

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